Received: Aug '22
Revised: Sep '22
Accepted: Sep '22

ANALYSIS OF THE DESIGN OF CMOS TWO-STAGE OPERATIONAL AMPLIFIER FOR THE SURVEILLANCE OF ECG SIGNALS

K Balaramudu [1] and Dr. Pramod Sharma[2]
[1]Research Scholar, University of Technology, Jaipur
[2]Professor, University of Technology, Jaipur

ABSTRACT

An innovative two-stage functional enhancer for biomedical applications is presented in this research. For low clamour, low power, high PSRR, and high CMRR, this two-stage is designed. For stable activity in critique mode, the Mill Operator Pay Strategy (Cc) is combined with a Mulling Dynamic Opposition (Rz) that is carried out using Transmission Entryway Semiconductors. Small Power A new problem in the ever-evolving gadget sector is scattering. The most prominent aspect of region contracting, which serves as the foundation for every contracted size when CMOS circuits are used in coordinated circuit production, has been noted. The semiconductor components of many CMOS Coordinated Circuits have a significant impact on usefulness in terms of rate, power scattering, and other factors. The largest plan boundaries in CMOS circuit design were previously anticipated to conduct advancement of the previously specified bounds, among other techniques. The CMOS-based IC design has significant constraints for idleness, power, and aspect.

Keywords: ECG signals, CMOS, Operational, surveillance, Two-Stage.

1. INTRODUCTION

Due to the reliability issue with small-size MOSFET semiconductors and the growing use of lightweight, long-lasting battery-operated handy electronic systems, low-voltage power sources for CMOS synchronised circuits are being used more frequently. Microelectronics' rapid advancement in recent years has led to an increase in the number of applications that call for a super low sufficient signal estimate module, such as implantable devices used in biomedical applications to monitor a few Neuro-solid exercises. Examining the biological indicators of the human body is a very fascinating topic since it frequently yields important information about the body's wellbeing. These details enable medical professionals to evaluate illnesses. Low voltage levels and low recurrence characterise biomedical signals like electrocardiograms (ECG), electromyograms (EMG), and electro-encephalogms (EEG). Table 1 lists these signs' characteristics.'

Signal	Frequency	Amplitude
ECG	0.05-250 Hz	5 uV-8 mV
EEG	0.5-200 Hz	2 uV-200 uV
EMG	0.01-10 KHz	50 uV-10 mV

Table: 1 The most popular biomedical signals

The functional speaker used in popular technology in a biological testing framework should exhibit extremely low-alluded disturbance, low power, and a high well-known mode dismissal proportion (CMRR). In this paper, a functional speaker with low voltage, low noise, and high CMRR is suggested for a flexible screen architecture. The functional enhancer has a high CMRR and can operate under 1-V stock as well.

The improvement of knowledge, small devices, and special equipment has significantly altered and improved the manner of life for an individual. In addition, the additional plan's possibilities show a more notable throughput and a longer battery lifespan. The semiconductor industry's confidence that it will follow Moore's Law for many more years to come is what allows for low-cost memory, enormous handling strength, and quick pack linking. As the CMOS device gets smaller, the circuit plan is implemented and disseminates low power. During the manufacturing process, ICs using 14nm manufacturing techniques are used. The investigation of circuit definition in 7nm manufacturing processes is done by IC makers. EDA-based technologies assist in identifying the best detailing strategies for reducing power consumption while also reducing the component of door measuring and VT decision. Engineers invest a lot of time and energy on programming decisions in order to come up with a solution to the detailed challenge.

2. REVIEW OF LITERATURE

The methodology's simplicity and ease make the development of VLSI circuits necessary for new

methods. In the study published by Sarkar et al. (2018), the goal of accomplishing this element is ideal, and the Whale Enhancement Calculation is used to achieve decreased balanced voltage in the definition of two-step CMOS Overpowered amp. The proposed plan will be taken into consideration as extra circumstances in the functional speaker's plan if it complies with specific detailing standards, including Slew Rate, Open Circle Acquire, and others. It is believed that balance decline is crucial for tracking current uniqueness during the Functional Intensifier's result phase.

This method of reformulating the Functional Enhancer in the standard Rhythm Virtuoso circuit test system allows for the validation of the cycle's customised results. The results achieved using the Whale Advancement Strategy and the replicated results may be easily distinguished from one another. The conclusions drawn by the proposed WOA are then evaluated in light of the applicability of a variety of different strategies used in past exploratory investigations. As analysed utilising various approaches, it can be seen that the WOA was able to provide better results for the circuit aspect with the most compact design in the CMOS Functional Enhancer plan for lower offset. A thorough analysis reveals that WOA surpasses all other methods by obtaining a quicker blending, the least amount of power dispersal, and the least amount of offset.

Simple ICs are given a boost in terms of dependability, utility, and expense sufficiency using electronic plan methods. It is feasible to accurately establish the fundamental strength of the sign at a circuit in the event of aggravation restrictions, but doing so makes the circuit design more challenging. When employing streamlining solutions, it takes a long time to find the arrangements and sophisticated cycles that manage a greater variety of competing restrictions or configuration needs and a wider territory of characteristics in the Configuration process. To get beyond the aforementioned restrictions, Singh et al. (2018) propose the Molecule Multitude Streamlining with a Maturing Pioneer (ALCPSO)- subordinate detailing technique. The simultaneous lowering of heated commotion and the circuit component was the scientists' clear focus in the proposed effort. To do this, the configuration inside the area that is intended to manage the scenarios and the characteristics that are significant in the circuit's fine-grained details are examined using ALCPSO.

However, the intended strategy for determining the circuit contains other elements that are absent in the previous automated method, as well as reduction in bending owing to heated impact as one of the unambiguous plan conditions. Reduced length and width minimise the area of the circuit, which is the goal of the design process. The ALCPSO-plan strategy's evaluation was carried out using MATLAB. Utilizing the ALCPSO approach to orchestrate in the Rhythm device with 0.18 m boundaries, the suggested solution is explored.

3. TWO STAGE CMOS OP-AMP BLOCK DIAGRAM

Some straightforward circuit designs are supported by functional intensifiers. These circuits' accuracy and speed depend on the operation amp's transfer rate and DC acquisition.

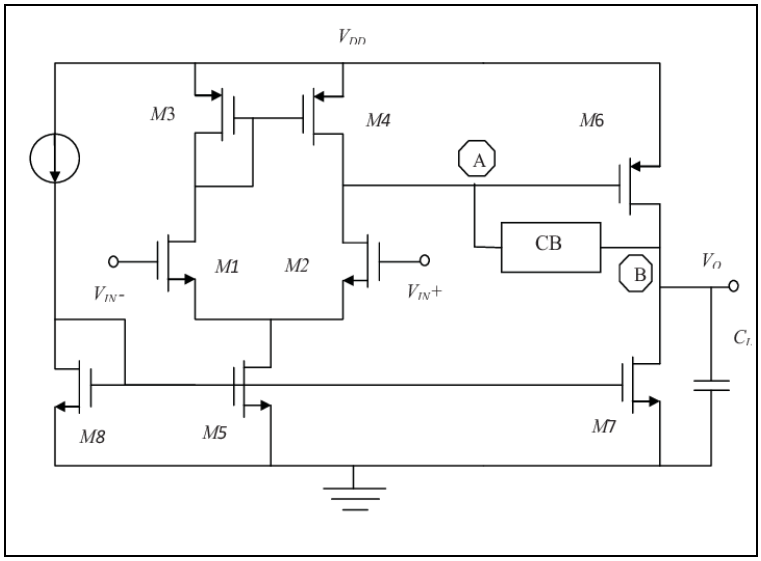

Figure: 1 Block diagram two stage CMOS Op Amp

Greater data transfer capacity and gain will result in an intensifier that operates more quickly and precisely. Figure above depicts the general block diagram of an operation amp with a result cushion (1).

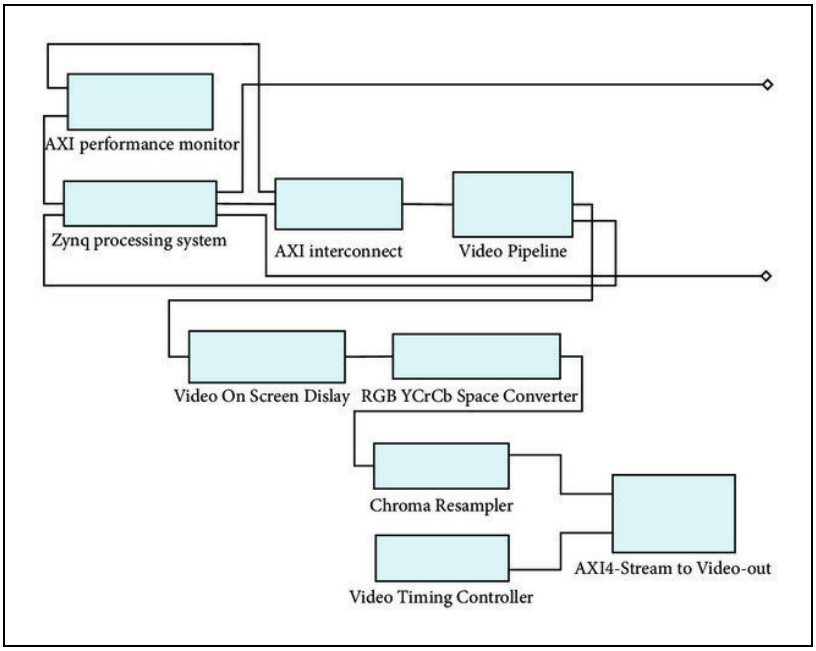

Figure: 2 Simplified Block Diagram

Figure shows the Block Chart that was created (2). A differential speaker makes up the initial block. It has two data sources, the non-rearranging voltage and the converting voltage. It produces a differential voltage or current that solely depends on a differential information voltage as a result. A differential finished to single finished converter is the next block. The original block's differential signal is transformed into a single final yield signal. Some engineering doesn't require the differential to complete a single capability, so this block may be eliminated in such case.

In circuits where the addition provided by the information stages is insufficient, a continuous enhancement is needed. One such enhancement is the normal source intensifier, which is powered by the primary stage yield. As a result of this stage's use of imbalanced yield differential intensifier, it provides the necessary additional increase. The biassing circuit is present to provide each semiconductor in its immersion region with the proper operating point. The result support stage provides the low impedance at yield and higher result current needed to power the multitude of operating amps or continue to increase the high number rate. Since a sizable portion of applications don't require low result impedance, even the result stage can be eliminated. A yield cradle is not required if the operation amp is only anticipated to drive a small, simple capacitive load. When the result stage is not in use, the circuit operates as a trans conductance speaker, or OTA. The pay circuit is designed to reduce addition at high frequencies and maintain security when negative input is applied to the operating amplifier.

4. ECG DATA ACQUISITION SYSTEM

The initial step in securing ECG data is the adoption of skin-connected terminals. Three cathodes are used as sensors to differentiate the heartbeats coming from a human body. Two terminals each go to the left and right wrists, while the third terminal goes to the lower leg of the ground leg. The observed ECG signal has a range of 5 uV to 8 mV. Due to the low voltage, the sign is handled in an intensifier circuit where it is raised to a positive voltage level. The enhancer's yield is then handled by a band pass channel circuit and a High Q indent channel.

This channel's function is to separate the exceedingly low and high recurrence commotion sections of the signals from the 60-Hz power line impediment. After being transferred to S/H and ADC, the channel's positive simple result becomes a computerised signal. From that point on, these sophisticated data will be managed by laptops or chips. The structure for acquiring ECG information is shown in Figure.3.

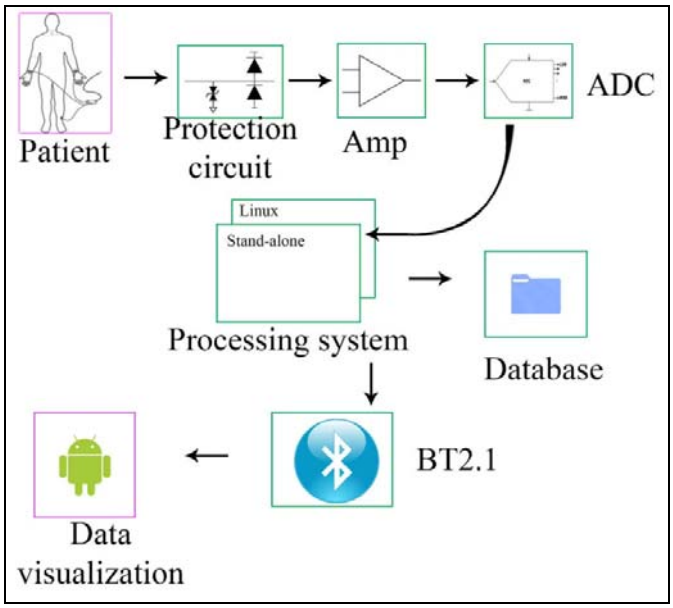

Figure: 3 ECG Data Acquisitions

5. ECG SIGNAL

The electrocardiogram (ECG) signal plays a critical role in identifying and diagnosing heart conditions. The tiny electric waves generated by the beating of the heart are captured on an electrocardiogram. The identification of the complex QRS and the evaluation of the fast pulse are the basic tasks in the ECG signal analysis. Figure 2 is an example of a typical ECG pattern, which includes a P wave, a QRS complex, and a T wave.

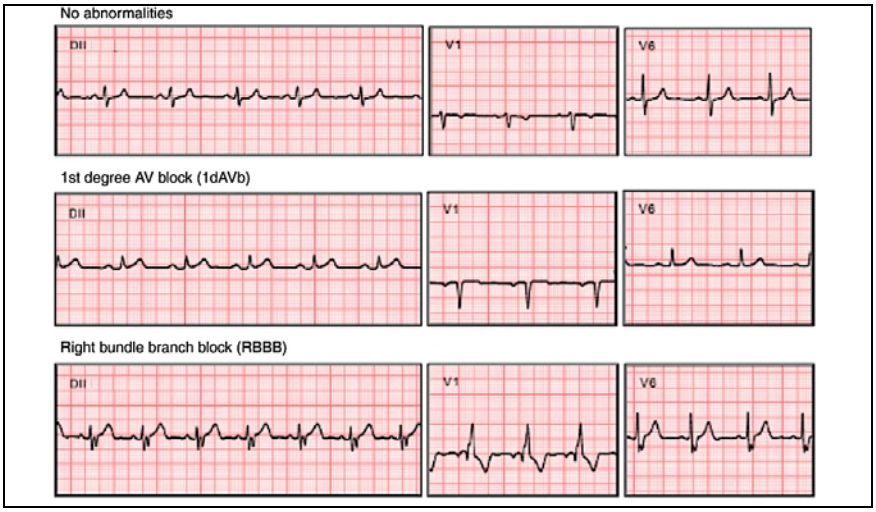

Figure: 4 Shows an Example of a Normal ECG Trace

The contractions of the atria are represented by the P wave, and those of the ventricles are represented by the QRS complex. A heartbeat is indicated by the R peak. In an ECG, the T wave is the final common wave. When the ventricles repolarize, an electrical signal is generated

The heart has four chambers and is a solid syphon. The two bottom chambers are known as ventricles, and the two upper chambers are known as atria. We have obtained information from the MIT-BIH Arrhythmia Data collection for the preparation and testing of the suggested ECG enhancer Plan. A characteristic electrical framework causes the heart muscle to agree and syphon blood via the heart to the lungs and the rest of the body. View the information (VIN) ECG signal in Figure 4.

6. ECG ENHANCER PLAN

An ECG signal typically varies from 5uV to 8mV. It is predicted that the enhancer will boost this weak signal to a usable level. The key speaker for biological applications is shown in Figure 4. The

functional intensifier is designed using this two-stage approach, where the first stage is a differential info pair and the second is an increase stage. It contains a mulling dynamic resistor and a mill operator compensation capacitor (Cc) (Rz). Because the biological signal is so weak, the bustle will have an impact on it. Due to the low occurrence of biological sign, the glint clamour heavily depends on the length and breadth results of a CMOS semiconductor. The glimmer clamour is depicted in Eq. (1), and the semiconductor region, WL, corresponds to the glimmer clamor's phantom thickness. Larger devices may generally be less susceptible to 1/f commotion. But using huge PMOS semiconductors, the information pair (M1 and M2) of the information stage was planned. The information stage makes use of a P-channel current source (M5) and an n-channel current mirror load (M3 and M4).'

$$V_n^2 = \frac{K}{C_{OX}WL}.\frac{1}{f}$$

The second phase of the functional intensifier employs an n-channel normal source intensifier (M6) with a p-channel current source load (M7). Due to the high result protection of these two semiconductors (M7, M6), the overall speaker gain and this stage gain are both considerably and reasonably significant. The information opposition is basically endless because the doors of MOS semiconductors are coupled to the functional intensifier inputs. The semiconductors' specifications were created to support a sufficient result voltage swing, yield offset voltage, slew rate, and acquisition data transfer item at a tilt current of 0.5 A.

6.1. Current Mirrors

Current mirrors are often utilised in MOS simple circuits as dynamic loads and biassing components to obtain high AC voltage gain. Since the edge voltage (Vth) drop makes the channel to source voltage (VDS) more significant than the entryway to source voltage (VGS), improvement mode semiconductors stay submerged when the entryway is linked to the channel.

$$V_{DS} = V_{GS} - V_{Th}$$

According to Eq. (2), constant current sources are obtained by current mirrors designed by running a reference current through a semiconductor that is associated with a diode (a door attached to a drain).

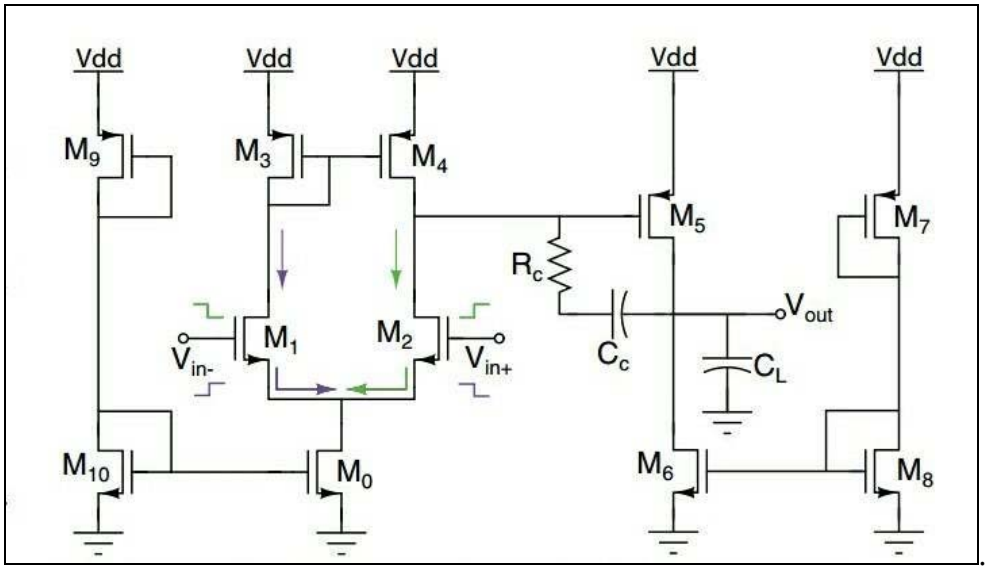

Figure: 5 Schematic of Two-stage Operational Amplified

We select a straightforward current mirror since it runs at low voltage (1-V). The designs for PMOS and NMOS current mirrors are shown in Figures 5(a) and (b), respectively. A PMOS reflect acts as an ongoing supply, whereas the NMOS acts as an ongoing drain. The voltage produced across the semiconductor connected to the diode is applied to the entrance and wellspring of the subsequent semiconductor, resulting in a constant result current. Due to the fact that both semiconductors have a similar entrance to source voltage, the flows when the two semiconductors are in the immersion district of activity are characterised by the following equations (Eqs.

7. RESULT

7.1. Device Parameter

The device parameters for a two-stage operational amplifier are shown in Table 1.

Table:1 Two-stage amplifier device parameters

Device	Type	W(um)	L (um)
M1,M2	**P**	**20**	**410**
M3,M4	**N**	**28**	**659**
M5,M8	**P**	**45**	**580**
M7	**P**	**90**	**640**
M6	**N**	**25**	**200**
M9	**N**	**5**	**200**
M10	**P**	**20**	**200**
M11	**N**	**6**	**900**

7.2. Recurrence Reaction, Pay

Single-stage remotely redressed and two phase inside repaid enhancers, both of which can have a two post type recurrent reaction, are the two most popular forms of functional intensifier designs. Figure 8's overall two posts, one zero little signal identical circuit can display the two phase speaker's little sign conduct while omitting upper request posts. The information stage model in Figure 4 (without (Cc) and (Rz)) has two hafts: Eq. (7) and Eq (8)

$$P_1 = \frac{1}{C_1 \frac{1}{g_{m3}}}$$

$$P_2 = \frac{1}{C_2 (r_{02} r_{04})}$$

A shaft splitting capacitor can be used to complete the two phase CMOS enhancer's payment. To achieve a stage edge that is more noticeable than 45 degrees is the goal of the pay task. If the potential non-prevailing shafts on the circuit are disregarded, the circuit can be roughly addressed by the little sign similar circuit of Figure 8 (without Rz).

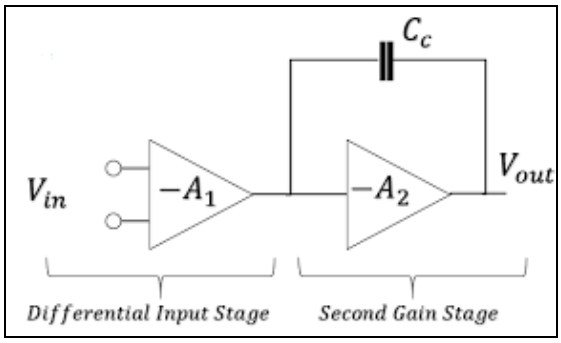

Figure: 6 Basic Two Stage Op-amp Simplified Small Signal Model Added with the Nulling Resistor

The circuit depicts two shafts and a half in the right plane zero, which, assuming that they are generally isolated, may be shown to be roughly located at (Eqs (9), (10) and (11), respectively). The circuit displays a right plane zero with two and a half shafts, which, assuming that they are generally separated, may be shown to be roughly located at (Eqs (9), (10) and (11)).

$$P_1 = \frac{-1}{(1 + g_{m2} R_2) C_c R_1}$$

$$P_2 = \frac{-g_{m2} C_C}{C_2 C_1 + C_C C_1 + C_2 C_C}$$

$$Z = \frac{g_{m2}}{C_C}$$

It should be noted that the mill operator impact in the stage after has pushed the shaft because of the capacitive stacking of the main stage continuously, p1, down to an exceptionally low recurrence, while the post because of the capacitance at the result hub of the second stage, p2, has been pushed to an exceptionally high recurrence because of the shunt criticism. Thus, shaft separation is the name of the compensation strategy.

8. CONCLUSION

This study included the whole design and analysis of a two-stage CMOS operating amplifier. The

outcomes show that the suggested intensifier met each component of the advance plan in a successful manner. The ECG Checking Framework, a two-stage functional enhancer created for low voltage and low power applications, is presented in this study. Applications requiring low power, low voltage, high CMRR, and high PSRR, including small battery-operated devices and biomedical instruments, are well suited for this two-stage enhancer with mill operator compensation. The circuit of a Phantom was created using 0.90um CMOS technology. Because flash commotion differs from that of N-channel input devices with P-channel load, we employed P-channel input devices with N-channel load to reduce enhancer commotion.

REFERENCES

1. C. Bronskowski and D. Schroeder, "An ultra low–noise CMOS Operational Amplifier with programmable Noise-Power Trade-off", IEEESolid-State Circuits Conference, (2006), pp. 368 - 371
2. C. Ken and L. Xiaoying, "A Zigbee Based Mesh Network for ECG Monitoring System", Bioinformatics and Biomedical Engineering (iCBBE), (2010), pp.1-4.
3. C.-C. Huang, S.-H. Hung and J.-F. Chung, "Front-End Amplifier of low-Noise and Tunable B/W Gain for Portable Biomedical Signal Acquidition", IEEE Circuits and Systems, (2008), pp. 2717 – 2720.
4. C.-T. Ma, P.-I. Mak, M.-I. Vai, P. Mak, S.-H. Pun, W. Feng and R.P. Martins, "A 90nm CMOS Bio-Potential Signal Readout Front-End with Improved Powerline Interference Rejection", IEEECircuits and Systems, (2009), pp. 665-668.
5. D. Popovic, B. Stein, R. B. Jovanovic, K. L. Dai, A. R. Kostovand and W.W. Armstrong, "Sensory nerve recording for closed-loop control to restore motor function", IEEE Trans. Biomed.Eng, vol. 40, no. 10, (1993), pp. 1024-1031.
6. D.Yates, E. Lopez-Morillo and R.G. Carvajal, "A Low-Voltage Low-Power Front-End for wearable EEG Systems", Conference of the IEEE EMBS, (2007).
7. Garbaya, A., Kotti, M., Drira, N., Fakhfakh, M., Tlelo-Cuautle, E., & Siarry, P. (2018, May). An RBF-PSO technique for the rapid optimization of (CMOS) analog circuits. In Modern Circuits and Systems Technologies (MOCAST), 2018 7th International Conference on (pp. 1-4). IEEE
8. H.-C. Chow and B.-S. Tang, "A high Performance Current-mode Instrumentation Amplifier for Biomedical applications", 2 nd International Conference on Signal Processing Systems, (2010).
9. J.G. Webster, "Medical instrumentation: Application and design", 3rd ed, John Wiley & sons Inc,(1998).
10. Lentola, A. Mozzi, A. Neviani, A. Baschirotto, "A 1uA Front-End for Pacemaker Atrial Sensing Channels", IEEE , (2009).
11. M. Swan, K. Arabi and B. Provost, "Implantable volume monitor and miniaturized simulator dedicated to bladder control", Artificial Organs, vol. 21, no. 3, (1997), pp. 219-222.
12. M.F.Li, Uday Dasgupta, X. W. Zhang and Yong Ching Lim, "A Low-Voltage CMOS OTA with Rail-to-Rail Differential Input Range", IEEE Transactions on circuits and systems, (2000) January, vol 47, pp.1-8.
13. Mallick, S., Kar, R., Mandal, D., & Ghoshal, S. P. (2017). Optimal sizing of CMOS analog circuits using a gravitational search algorithm with particle swarm optimization. International Journal of Machine Learning and Cybernetics, 8(1), 309-331.
14. R. Stein, B. Charles, D. Davis, L. Jhamandas, J. A. Mannard and T. R. Nichols, "Principles underlying new methods for chronic neural recording", Can. J. Of Neuro.SCI., (1975), pp. 235-244.
15. Sarkar, P., Laskar, N. M., Nath, S., Baishnab, K. L., & Chanda, S. (2018). Offset voltage minimization-based circuit sizing of CMOS operational amplifier using a whale optimization algorithm. Journal of Information and Optimization Sciences, 39(1), 83-98.
16. Singh, C. L., Anandini, C., Gogoi, A. J., & Baishnab, K. L. (2018). Automated sizing of low-noise CMOS analog amplifier using the ALCPSO optimization algorithm. Journal of Information and Optimization Sciences, 39(1), 99-111.
17. Singh, K., Jain, A., Mittal, A., Yadav, V., Singh, A. A., Jain, A. K., & Gupta, M. (2018). Optimum transistor sizing of CMOS logic

circuits using logical effort theory and evolutionary algorithms. Integration, the VLSI Journal, 60, 25-38.

18. T. H. Ning, P. W. Cook, R. H. Dennard, C. M. Osburn, S. E. Schuster and H.N. Yu, "1um MOSFET VLSI technology, Part IV-Hot-electron design constraints", IEEE Trans. Electron. Devices, vol. 26, (1979), pp. 346-353.
19. W.-S. Wang, Z.-C. Wu, H.-T. Huang and C.-H. Luo, "Low Power Instrumental Amplifier for Portable ECG", IEEE Circuits and Systems International Conference, (2009), pp. 1-4.
20. Y. Hu. and M. Sawan, "CMOS Front-end Amplifier Dedicated to Monitor Very low Amplitude Signal from Imlantable Sensors", Kluwer Academic Publishers, vol. 33, (2002), pp. 29-41.